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branch target address cache

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Branches interrupt the sequential flow of instructions and introduce pipeline bubbles.

Branch penalty can be a significant component of effective cpi ...

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In more parallel processor designs, as the instruction cache latency grows longer and the fetch width grows wider, branch target extraction becomes a ...

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We discuss the impact of different branch target caching policies and cache sizes on the efficiency of branch target address cache. ...

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Data processor with branch target address cache and method of ...

A data processor (10) has a BTAC (48) storing a number of recently encountered fetch address-target address pairs. Each pair also includes an offset tag ...

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In a branch instruction target address cache, an entry associated with a fetched block of instructions includes a target address of a branch instruction ...

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First ...

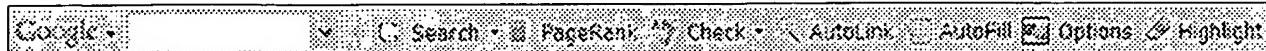
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tags yes branch target address cache BTB tags yes yes branch target buffer ...
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F Arakawa, T Yamada, T Okada, M Ishikawa, Y Kondo, ... - Systems and Computers in Japan, 2006 - doi.wiley.com

... which is the reason we did not adopt BTAC architecture. ... 6. Middleware relative performance of SH-X. ... an example of the clock activity control of a register file ...

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AP Scott, KP Burkhart, A Kumar, RM Blumberg, GL ... - Hewlett-Packard Journal, 1997 - docencia.ac.upc.edu

... If a branch hits in the BTAC but is predicted not ... its result is held in a temporary rename register and made ... Relative to the PA 7200, the misprediction rate is ...

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K Diefendorff - Microdesign Resources, Microprocessor Report, 1999 - ece.umd.edu

... Instead of a BTAC, some processors use a branch target instruction cache ... Register File ... however. Designed as shared multidrop buses for DRAM, I/O, and multiproces ...

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U Sigmund, T Ungerer - Journal of Universal Computer Science, 2001 - jucs.org

... thread executes in a separate architectural register set. ... thread); a 1024-entry branch target address cache (BTAC); ... in Figure 15 and the relative IPC decrease ...

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A Gara, MA Blumrich, D Chen, GLT Chiu, P Coteus, ... - IBM Journal of Research and Development, 2005 - research.ibm.com

... A branch target address cache (BTAC) reduces branch latency. ... each with its own arithmetic pipe and register file ... The relative size of the sections is adjustable ...

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D Hunt - Compcon'95.'Technologies for the Information Superhighway', ..., 1995 - ieeexplore.ieee.org

... As mentioned earlier, the BTAC avoids the taken branch ... bus, Store data is copied from the register file to the ... Loads and stores to the I/O address space and ...

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Mispredicted Path Cache Effects

P Amestoy... - Springer

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... It is also not obvious whether polymerized bilayers should be more or less permeable relative to their monomeric counterparts. ... CB 1 n || o=c c=o || cH3 ...

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S Yehia, N Clark, S Mahlke - Proceedings of the 2005 international conference on ..., 2005 - portal.acm.org

... a BRL has an entry in the **BTAC**, control is ... variety of sub- graphs, while maintaining a relative low interconnect ... 2. Each bit of the output register, r7, can be ...Cited by 1 - Related Articles - Web SearchResult Page: [1](#) [2](#) [3](#) [Next](#) [Google Home](#) - [About Google](#) - [About Google Scholar](#)

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